Amendments to the Specification:

On page 1, please replace the first line with the following amended paragraph:

-- TITLE OF THE INVENTION: Communications Apparatus

CROSS-REFERENCE TO RELATED APPLICATIONS.

This application is related to and claims priority from United Kingdom patent application number GB 19970018131 filed on August 27, 1997, the entire contents of which are hereby incorporated by reference, and from International Application number PCT/GB98/02583 filed on August 27, 1998, entitled "Communications Apparatus" by Radioscape Limited, the entire contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

(1) Field of the Invention--

On page 1, after the first paragraph, please insert the following heading:

-- (2) Description of Related Art --

On page 9, after the first full paragraph, please insert the following heading:

-- BRIEF SUMMARY OF THE INVENTION --

On page 11, after the first full paragraph, please insert the following heading:

-- BRIEF DESCRIPTION OF THE DRAWINGS --

On page 14, after the fourth full paragraph, please insert the following heading:

-- DETAILED DESCRIPTION OF THE INVENTION --

On page 30, please replace the paragraph containing the objected to informalities in lines 20 and 21 with the following amended paragraph:

-- As its name suggests, the main purpose of the IMU is to manage the interface between the personal computing device (PCD, 109 in FIG. 1) on which the driver modules reside, and the rest of the system. The bussed inbound signal 1109 from the ADC unit (107 in FIG. 1) is passed into a first-in first-out (FIFO) buffer memory unit 1110, which allows the effectively asynchronous data capture to be interfaced to the microprocessor [[1113]] 1133 and passed to the host PCD. It also prevents data being lost if the microprocessor [[1113]] 1133 should be busy. The FIFOs 1110 and 1114 can be controlled from the outside (namely, from the ADC and DAC units, respectively, 107 and 110 in FIG. 1), via the control bus 1120. The bus

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management unit (BMU) 1118 controls the flow of information to and from 1133 the control bus 1120 and the various sub-stages of the IMU, including a bussed connection 1121 to the microprocessor 1133 and various control lines. One set of controls 1142 drives the input port management of FIFO 1110 under the ultimate control of the ADC stage (107 in FIG. 1); another drives the output port management of FIFO 1114 under the ultimate control of the DAC stage (110 in FIG. 1). The output port to inbound FIFO 1110 is controlled by the microprocessor [[1113]] 1133 via line 1111, which allows the microprocessor [[1113]] 1133 to read samples off the FIFO 'queue' via bus 1108. --

On page 33, please replace the paragraph containing the objected to informalities in lines 4 with the following amended paragraph:

-- After any processing which may be required (as discussed above), inbound data is passed by the microprocessor 1133 to the input port of the FIFO buffer 1106 via bus 1107, with port control line 1136. This queue of received, digitised (and interleaved, in I/Q mode) samples is then read from the output port of the FIFO 1106 by interface protocol driver (IPD) 1103, via bus 1105, with port control line 1140. The IPD is responsible for dealing with the various control lines, voltage levels, handshaking and coding that are required by the particular PCD bus interface in use, under the control of the microprocessor 1133 via line 1135. For example, depending on the embodiment, IPD 1103 may implement any or all of: a small computer system interface (SCSI) interface driver, a PC memory card international association (PCMCIA) interface driver, a universal serial bus (USB) interface driver, a peripheral component interconnect (PCI) interface driver, an industry standard architecture (ISA) or extended industry standard architecture (EISA) interface driver, a RS423/232 interface driver, or a driver for any other high-speed interface with which modern PCD devices are now or come to be equipped. Clearly, the faster the interface the better, particularly if the system is to be used to acquire high-bandwidth signals. In such a case, the slower ports (such as the conventional serial RS423/232) will be entirely unsuitable unless only a small amount of signal is occasionally required, in which ese which case the adapter could buffer the signal prior to transfer. Furthermore, for best performance, the interface bus should be able to support the function of direct memory access (DMA), which allows data to be streamed into and from the memory of the PCD without the interaction of the main processor unit on the PCD. This type of arrangement has the advantage of producing much less load upon the PCD system. Indeed, in an alternative embodiment of the RF adaptor of the current invention, the input FIFO 1110 is able directly to pass information directly to the output FIFO 1106, and input FIFO 1131 is able to pass information directly to output FIFO 1114, to maximise throughput. In any case, the inbound information (together with clocking, interrupt and other

control lines which may be read and/or written by the IPD 1103) are passed via connection 1138 to the main memory bus of the PCD.--